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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,458	KWAK ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9 and 13-18* is/are rejected.

7)☒ Claim(s) *4, and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09182001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "R" and "Q1" of Fig. 1; and "Q4" – "Q6" of Fig. 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: It is believed "passive resistance" on line 12 of page 1 was meant to be --active resistance--, since that is the basic critical feature of the present invention. It is suggested the sentence "The source of...PMOS transistor Q13" on page 8, lines 12-13 be deleted for two reasons: 1) It is incorrect

since Fig. 3 clearly shows the gate of Q13 being connected to the drain of Q8, and 2) that particular gate/source relationship is already described on lines 10-11. Appropriate corrections are required.

Claim Objections

Claim 11 is objected to because of the following informality: As presently written, the "a sum of voltages each...corresponding one" can be confusing. For example, it appears that "each" could refer either to "sum" (thus implying there might be more than just one sum of voltages), or to "voltages" (a plural term). Therefore, it is suggested the phrase be modified to read as --a sum of voltages, wherein each voltage is obtained between drain and source electrodes of a corresponding one-- to more clearly relate "each" to "voltages." An appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The limitations on lines 3-5 of claim 17 (i.e. "a source of the PMOS transistor...is connected to a gate of the PMOS transistor") are misleading and/or inaccurate because they appear to indicate the source of the PMOS transistor is actually connected to its gate, which does not accurately correspond to the applicants' own figures. For example, using the applicants' own Fig. 5 as a reference, Q31 corresponds to the claimed PMOS transistor, and Q17 corresponds to the first MOS transistor. If their connections are what the limitations within

claim 17 are supposed to correspond to, it is suggested claim 17's phrase "voltage and is connected to a gate of the PMOS transistor" be changed to --voltage,-- to more accurately relate the claimed structural limitations to the applicants' own figure. Otherwise, clarification is requested with respect to the source/gate connections of the PMOS transistor.

Claim 9 recites the limitation "the MOS transistor" in line 2 with insufficient antecedent basis for this limitation in the claim, or its chain of dependency. Was claim 9 meant to depend on claim 8 which does recite "a single MOS transistor"?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5-9, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Viehmann's PCT WO 01/61430 A1, (published in German on Aug 23, 2001). Fig. 2 shows one type of reference voltage generating circuit comprising active resistance part 22 having at least one MOS transistor 22, wherein the circuit is connected between external voltage U_{DD} and a ground voltage (not labeled). The gate electrode of MOS transistor 22 receives enable voltage U_E, which is understood to have a higher potential than the drain to source voltage of MOS transistor 22, thus allowing MOS transistor 22 to operate in a linear current-voltage region (e.g. see page 5, lines 5-15 with respect to "Drain-Source-Spannung…60 mV"; "Eingangsspannung zwischen 2 und 5 Volt"; "Gate-Source-Spannung…Eingangsspannung"; "als "linearer Bereich" oder "aktiver Bereich"." Therefore, claims 1-2 are anticipated. Interpreting the figure in a

slightly different manner, Fig. 2 shows a current mirror circuit 20,18 having first/second current paths 30,24,22/32,26 formed between first power source terminal U_{DD} and a second power source terminal (e.g. ground), wherein the current mirror circuit is operated in response to a voltage level of the second current path (i.e. via the voltage between 32 and 26 being applied to the gate of 30); reference voltage output node on the second current path (between 32 and 26) provides a reference voltage (e.g. see page 9, line 22 "Transistor 26 abfallende Spannungsabfall U_{26}"); and active resistance device 22, on the first current path, is operated in the linear region (as previously described). Therefore, claims 6, 8-9, and 13 are anticipated. MOS transistors 24 and 26, formed on the first and second current paths, respectively, control the current flowing in those paths, thus anticipating claim 14. Since the current mirror circuit includes a pair of PMOS transistors 30 and 32 formed on the first and second current paths, respectively, claim 15 is also anticipated. Although not shown in the figure, one of ordinary skill in the art would understand that enable (control) voltage U_E is supplied by some type of circuitry. Deeming that circuitry one type of a voltage supply circuit, claims 5 and 7 are anticipated.

[Note: Viehmann's U.S. Patent 6,586,919 B2 (filed Aug 15, 2002), is considered an acceptable English translation of the PCT reference used in the above rejections.]

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-9, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants' own Prior Art Fig. 2. The figure shows a reference voltage generating circuit connected between external voltage Evcc and ground. Although it shows resistance part R, it is not an active resistance part with at least one MOS transistor. However, it would have been obvious to one of ordinary skill in the art to replace (passive) resistance part R with at least one MOS transistor, wherein its gate would receive an enable (e.g. control) voltage at a potential higher than the drain-source potential, allowing the at least one MOS transistor to operate in a linear current-voltage region, thus rendering claim 1 obvious. The at least one MOS transistor would provide a means for allowing the user to adjust the resistance of the resistance part, to obtain the desired output voltage, by adjusting the voltage applied to the transistor's gate. Also, MOS transistor used as a resistive device also takes up less area than a discrete resistor. [Note: When a MOS transistor is used as a resistive device, it is typically used in its linear current-voltage region (also known as the triode, resistive, ohmic or non-saturation region).] It would have been obvious to replace resistive part R with a single MOS transistor, rendering claim 2 obvious. The single MOS transistor could be used as a means to adjust the voltage applied to the gate of transistor Q7 to obtain the desired reference voltage Vref, and also be used in place of a

resistor that requires more area. It would have been obvious to one of ordinary skill in the art to replace resistance part R with a plurality of series coupled MOS transistors, thus rendering claim 3 obvious. The plurality of MOS transistors would provide one type of means for adjusting the gate voltage of Q7. For example, the plurality of MOS transistors would provide more of a variety with respect to the resistance (voltage) adjustment, wherein each MOS transistor could be controlled individually and the voltage drops across the different resistances would be summed to provide a desired, precise voltage to Q7's gate. It would have been obvious to one of ordinary skill in the art to use a voltage supply circuit for supplying the enable voltage to the at least one MOS transistor, rendering claim 5 obvious. The voltage supply circuit could be used to provide the desired control (enable) voltage, thus providing the ability to separately adjust the active resistance part (e.g. the at least one MOS transistor) when necessary. Re-interpreting the applicants' Prior Art Fig. 2 in a slightly different manner, it shows current mirror circuit Q4-Q7, R having first/second current paths Q4,Q6,R/R5,Q7 formed between first power source terminal Evcc and second power source terminal (ground), wherein the current mirror circuit is operated in response to a voltage level of the second current path (i.e. via voltage Vref applied to the gate of Q6); an unlabeled reference voltage output node, located on the second current path, provides reference voltage Vref; and resistance device R. Applying the same reasoning as previously described with respect to claims 1-3 and 5, claims 6-9 and 13 are rendered obvious because at least one single MOS transistor could be used in place of resistance device R. MOS transistors Q6 and Q7, formed on the first and second current paths, respectively, control the current flowing in those paths, rendering claim 14 obvious. Since the current mirror circuit includes a pair of PMOS transistors Q4 and Q5 formed on the first and second current paths, respectively,

claim 15 is also rendered obvious. Re-interpreting the applicants' Prior Art Fig. 2 in still another way, first/second MOS transistors Q4/Q5 comprise a current mirror circuit receiving externally applied voltage Evcc; third/fourth MOS transistors Q6,Q7 comprise a current control circuit; and resistance circuit R. As previously described, it would have been obvious to one of ordinary skill in the art to replace resistance circuit R with at least one (a fifth) MOS transistor as a means to allow adjustment to the circuit. The fifth MOS transistor would function as an active resistance circuit, and since it would be coupled to ground, would typically be an NMOS transistor. With an NMOS transistor used as the fifth MOS transistor, in place of resistance circuit R, the modified circuit with first-fifth MOS transistors corresponds to the transistors Q8,Q9,Q11,Q10, Q12 shown in the applicants' own Fig. 3. Due to this direct correlation, it is not considered necessary to describe the specific MOS transistor connections (i.e. gate, drain, and source). To operate as a resistance device, the control (gate) voltage of the fifth MOS transistor would be higher than the drain to source voltage of the fifth MOS transistor. Therefore, claim 16 is rendered obvious.

Allowable Subject Matter

Claims 4, and 10-12 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the gate electrodes of the MOS transistors (connected to a common node in claim 4) receive the enable voltage as recited within claims 4 and 10 (upon which claim 11 depends); or 2) the voltage supply circuit includes one PMOS transistor and a plurality of NMOS transistors as recited within claim 12.

Also, claims 17-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Similar to claim 12 described above, there is presently no strong motivation to modify or combine any prior art reference(s) to ensure the voltage supply circuit has at least one PMOS transistor and a set of NMOS transistors as recited within claim 17 (upon which claim 18 depends).

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although none of the references were cited within any of the formal prior art rejections described above, it is believed each reference could have been used to reject at least some of the basic claims. The circuits of Chiu could be considered types of reference voltage generating circuits, wherein Fig. 3 shows active resistance part MN_R, which is disclosed as being operated in the triode (e.g. linear current-voltage) region (e.g. see column 2, lines 43-45). Also, this reference clearly discloses that a resistor in prior art circuits can be replaced by a MOS transistor operating in the non-saturation or triode region to use less area (e.g. see column 1, line 66 through column 2, line 1). O'Shaughnessy et al. clearly teaches MOS transistors operating in the ohmic region can be used as a voltage controlled variable resistor, which can also be used as a precision resistor (e.g. see column 3, lines 28-48). Circuit 20,10, shown in O'Shaughnessy's Fig. 2, can be considered one type of reference voltage generating circuit wherein the voltage on VIN+ is the reference voltage, 10 is active resistance part R1 with MOS transistor N operated in a linear current-voltage region in response to enable (control) signal VG provided by supply voltage circuit 22. Hwang et al. shows an example of a

circuit wherein a resistor R (see 102 in Fig. 1) is replaced by a single MOS transistor (see 202 in Fig. 2) that receives enable (control) voltage VG at its gate, wherein the transistor is disclosed as operating in the triode region (e.g. see column 1,lines 28-31). Therefore, all of these references should be carefully reviewed and considered.

The prior art references cited on the IDS submitted Sep 18, 2001 were reviewed and considered. None of these references clearly discloses an active resistance part having at least one MOS transistor operating in the linear current-voltage (e.g. triode, linear, ohmic, or non-saturation) region as recited within each independent claim.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
1 September 2004

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